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APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Date-Gun Lee**, a citizen of Korea, residing at 310-801, Seolak Maeul, Jung-dong, Wonmi-ku, Bucheon-city, Kyungki-do, 420-020, Korea have invented a new and useful **METHODS TO FABRICATE A SEMICONDUCTOR DEVICE**, of which the following is a specification.

METHODS TO FABRICATE A SEMICONDUCTOR DEVICE

FIELD OF THE DISCLOSURE

[0001] This disclosure relates generally to semiconductor devices, , and more particularly to methods to fabricate a semiconductor device.

BACKGROUND

[0002] When two or more layers are deposited and the upper layer is to be etched during the fabrication of a semiconductor device, an end point detection (EPD) system is generally used in the etching process. The EPD system sets an etch stop point (e.g., the point at which the lower layer is exposed when etching the upper layer).

[0003] However, it is difficult to determine the etch stop point using the lower layer by the current EPD system for hole etching process, (which is used for forming contact holes or via holes), because the area exposed by via holes is small, (e.g., under 5% of the whole wafer area). Therefore, conventional time etching is used instead.

[0004] Figs. 1a and 1b are sectional views illustrating a conventional hole etching process for a semiconductor device. As shown in Fig. 1a, an interlayer insulating layer 1, in which holes will be formed, is first formed. A nitride layer 2, which will be used as a hard mask, is formed on the interlayer insulating layer 1. A photoresist pattern 3 is formed on the nitride layer 2. The nitride layer 2 is etched using the photoresist pattern 3 as a mask to form a nitride layer pattern 4 as shown in Fig. 1b.

[0005] Subsequently, the interlayer insulating layer 1 is time-etched using the nitride pattern 4 as a mask to form holes 5. The etching time, which is set for the hole formation, is determined by considering the etch rate of the interlayer insulating layer 1.

[0006] However, the time-etching is based on a premise that the conditions or state in a chamber are always the same. Therefore, there is a problem that the interlayer insulating layer cannot be etched to a desired extent if there is a change in the etch rate of the etching chemical or if there is a change in the thickness of the interlayer insulating layer after the CMP.

[0007] Prior art references dealing with the subject matter of the etch stop layer include the following US patents.

[0008] US Patent 6,383,943 describes a method of resolving a problem of discontinuous deposition of an adhesive layer at the bottom of via holes due to a notch of the silicon nitride etch stopper. US Patent 6,040,619 describes a formation method for a tungsten Damascene interconnect of a device using silicon nitride having a large amount of silicon as an etch stopper. US Patent 6,063,711 describes a method of forming a thin etch stop layer including oxynitride having large etching selectivity to oxide layer and preventing the etch stop layer from cracking. US Patent 6,245,663 describes a method of forming a thin etch stop layer by forming a dielectric etch stop layer after a metal CMP process instead of before the metal CMP process to prevent the etch stop layer being trimmed during the CMP. US Patent 5,612,254 describes a method of forming an interconnection inside the prepatterned

channel in a semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figs. 1a and 1b are cross-sectional views illustrating a prior art hole etching process of a semiconductor device.

[0010] Figs. 2a-2e are cross-sectional views illustrating a hole etching process of a semiconductor device performed in accordance with the teachings of this disclosure.

[0011] In the drawings, the thickness of layers and regions are exaggerated for clarity.

DETAILED DESCRIPTION

[0012] Figs. 2a-2e are cross-sectional views illustrating a hole etching process of a semiconductor device performed in accordance with the teachings of this disclosure. As shown in Fig. 2a, a nitride layer 12 is first formed on an interlayer insulating layer 11 in which contact holes or via holes will be formed. The nitride layer 12 serves as a hard mask during a subsequent hole etching process. It is preferable that the thickness of the nitride layer 12 is about 200-800 Å, for example, about 500 Å.

[0013] Then, a photoresist layer is formed on the nitride layer 12. The photoresist layer is exposed and developed to form a photoresist pattern 13. The photoresist pattern 13 will be etched together with the interlayer insulating layer 11 during a subsequent process. Therefore, the thickness of

the photoresist pattern 13 is determined by considering the thickness and etch rate of the interlayer insulating layer 11 and the etch rate of the photoresist pattern 13.

[0014] Next, as shown in Fig. 2b, the nitride layer 12 is etched using the photoresist pattern 13 as a mask. The photoresist pattern 13 is not removed, but remains after etching the nitride layer 12. Subseqeuntly, the interlayer insulating layer 11 is etched using the photoresist pattern 13 as a mask as shown in Fig. 2c.

[0015] As described above, the photoresist pattern 13 is etched together with the interlayer insulating layer 11 during an interlayer insulating layer etching process. This etching process is terminated by setting the time point when the photoresist pattern 13 is entirely removed such that the nitride layer 12 is exposed by the etching process as an etch stop point, as shown in Fig. 2d.

[0016] As stated above, the photoresist pattern 13 is not removed when the nitride layer 12 is etched, but rather remains after etching the nitride layer 12. Further, the etch rate of the interlayer insulating layer 11 is larger than that of the photoresist pattern 13. When the etch rate of the interlayer insulating layer 11 is about 5000 Å/min and that of the photoresist pattern 13 is about 1800 Å/min, the interlayer insulating layer 11 is formed to have about 7500 Å thickness and the photoresist pattern 13 after etching the nitride layer is formed to have about 2500 Å thickness. As a result, the photoresist

pattern 13 is entirely removed when the interlayer insulating layer 11 is etched about 7000 Å, thereby exposing the nitride layer 12.

[0017] Therefore, the EPD system is applicable in hole etching process by setting the exposing point of the nitride layer 12 as the etch stop point. If the EPD system is applied, it is preferable that the thickness of the photoresist pattern 13 is about 2500-3500 Å.

[0018] If it is desired to set the etch stop point as the point at which the interlayer insulating layer 11 is etched about 90%, the thickness of the photoresist pattern 13 should be smaller than the pre-determined value. On the other hand, if it is desired to set the etch stop point as the point at which the interlayer insulating layer 11 is completely etched, the thickness of the photoresist pattern 13 should be larger than the pre-determined value.

[0019] Subsequently, as shown in Fig. 2e, the interlayer insulating layer 11 is over-etched using the nitride layer 12 as a mask. Then, holes 14, (which may be used as contact holes or via holes), are completed in the interlayer insulating layer 11.

[0020] As described above, since an EPD system is applied to the hole etching process, the hole etching process can be performed to a uniform extent by the EPD system even if etching chemicals having different etch rates are used or if the thickness of the interlayer insulating layer 11 is changed after the CMP. In addition, various hole etching depths might be performed because the etch stop point is set at a desired point by controlling the thickness of the photoresist pattern.

[0021] From the foregoing, persons of ordinary skill in the art will appreciate that uniform hole etching can be performed regardless of etch rate changes of etching chemicals or thickness changes of the interlayer insulating layer after a CMP.

[0022] From the foregoing, persons of ordinary skill in the art will further appreciate that fabrication methods using an EPD system in an etching process have been disclosed. These methods enable uniform hole etching regardless of changes in the etch rates of the etching chemicals and/or the thickness of the interlayer insulating layer after CMP.

[0023] The illustrated fabrication method comprises: forming a nitride layer on an interlayer insulating layer; forming a photoresist layer on the nitride layer; exposing and developing the photoresist layer to form a photoresist pattern; etching the nitride layer using the photoresist pattern as a mask and contiguously etching the photoresist pattern and the interlayer insulating layer together; setting the etch stop point as the point that the photoresist pattern is removed by etching and, thus, the point at which the nitride layer is exposed.

[0024] After exposing the nitride layer by removing the photoresist pattern, the interlayer insulating layer may be over-etched using the nitride layer as a mask

[0025] It is preferable that thickness of the nitride layer is about 200-800 Å, and that the thickness of the photoresist pattern is about 2500-3500 Å.

[0026] Although certain example methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto.

On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.